

# Multi Controller Based High Efficient System with DVFS and DPM Control

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**ABSTRACT:** Normally embedded systems are energy constrained. Moreover, Low energy consumption and fault tolerance are often key objective in the design of real-time embedded system and for product success. To reduce the development time and cost, now a days its tendency to use commercial off-the-shelf (“COTS”) devices for complex embedded system. Real time devices usually use system level energy reduction method, dynamic voltage and frequency scaling (DVFS) and dynamic power management (DPM) are one of the most effective techniques for energy reduction. While in most of the COTS processors used system don’t have DVFS or apply DVFS only to processor cores. In this paper, a smart and versatile platform for low energy embedded systems is presented. To achieve energy saving, as it is main concern, we have applied DVFS to the whole microcontroller. The two microcontrollers are connected such that they can interrupt, restart, and turn on/off each other by DPM technique. Also we have shown that how easily we can control the power of each microcontroller and make them automated. With the help of GSM it is shown that how the system is advanced to save the energy as it supply the power to GSM only when needed. Also The Physical experiments show that applying DVFS on the whole microcontroller improve energy saving compared with the sole use of dynamic power management and applying DVFS only on the core, respectively.

**KEYWORDS:** Embedded System, Voltage and Frequency scaling, Power Management, etc.

## I. INTRODUCTION

Embedded systems are omnipresent, and they are highly preferred by the designers. Many of the embedded system are powered by the battery sources. Because of these it is not so easy for these types of system to charge or replace the power source frequently. That is why low power consumption is the key objective of this project. This project will be helpful for the devices like robot and hand held devices like digital camera, cell phone and mobile medical care devices. In today’s highly competitive embedded systems markets and early launching of products in the market with multiple requirements mostly commercial off-the-shelf (COTS) devices is affordable in designing the embedded systems. Many vendors offer reconfigurable hardware solutions to improve the manufacturing process and facilitate with variety of programmable logic device (PLD)-based evaluation kits. In addition, these system permits to test the SOC or ASIC devices on manufacturing. Embedded systems includes microcontroller that have a microprocessor with memory elements and I/O devices on a single chip. However the microcontroller doesn’t provide facilities to evaluate the energy management techniques.

In this paper, to meet the objective of embedded systems, we propose a platform for experimenting with energy management techniques (DPM and DVFS)

In Compares with earlier related works, how this platform is different and useful is shown below.

- 1) **This system provides DVFS strengths for the microcontrollers, including the processor cores, PLL, memory, and I/O units; On the other hand many existing designs either don’t have DVFS or apply DVFS only to processor cores, while our research in this paper shows that applying DVFS to PLL, memory, and I/O is beneficial;**

- 2) The system also have circuitry to measure energy consumption of different parts of microcontroller separately, including the processor core, PLL, memory, and I/O; with this technique it is easy to evaluate most power consuming parts of the controller.
- 3) The system is general and based on an ARM; therefore it can be used for many other types of existing microcontrollers and many other COTS devices.

## II. HARDWARE PLATFORM ARCHITECTURE

ARM7TDMI is the widely used COTS processor in instantaneous embedded systems as it is cheap, good performance and adaptable processor. Some vendors manufacture microcontroller by combining the ARM7TDMI processor with internal memory devices and various types of I/O devices on a single chip. It is remarkable that the computational power of ARM7 is good enough for the commonly used embedded applications. However, for high computational applications, the performance of ARM7 may not be tolerable. In such case, this proposed platform is not completely depending on ARM7. Any processor which allows variable frequency and variable supply voltage can be used in the designing of this proposed system.

The Hardware system includes a pair of AT91SAM7x256 microcontrollers connected via a bus. Based on the features of AT91SAM7x series, this bus can be easily designed as 16-bit parallel bus or SPI, UART, etc. AT91SAM7x256 have ARM7TDMI processor with 64-KB of SRAM, 256-KB of Flash memory, In-circuit emulation (ICE) and debug communication channel support. Two distinct power supplies are provided in the board to supply power to the I/O devices and the processor core of microcontrollers. Processor gives command to the power supplies and controls the power consumption of each part of the microcontroller. The concept of distinct supply voltages helps in both the analysis with various DVFS arrangements and to shut off either of processor to switch into a single processor operation mode. We can also choose random DVFS or DPM technique. The hardware platform is so flexible that we can extend it to measure the power consumption of the processor cores, PLLs, and I/O devices. Similarly, power consumption of the application running by the processors can also be evaluated. The report can be sent to the host computer via data logging port. Debugging facility is also provided for each microcontroller with the help of debugging ports [RS232 and Joint Test Action Group (JTAG) ports]. The hardware platform can be modified for a definite application, after evaluating the system in every aspect.

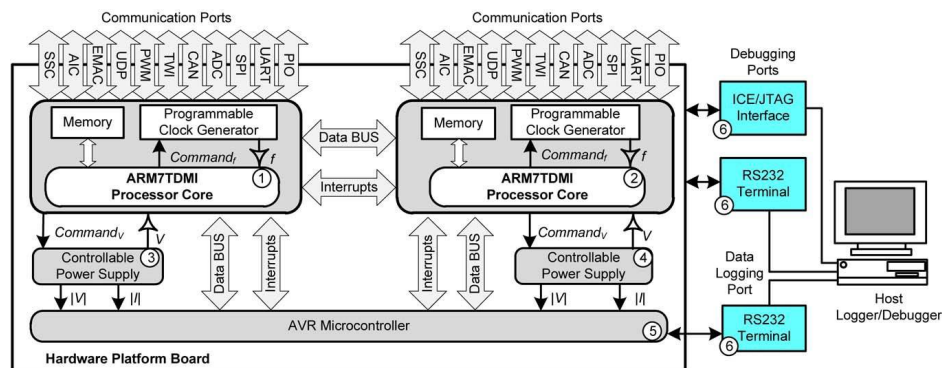


Fig. 1 Hardware Platform

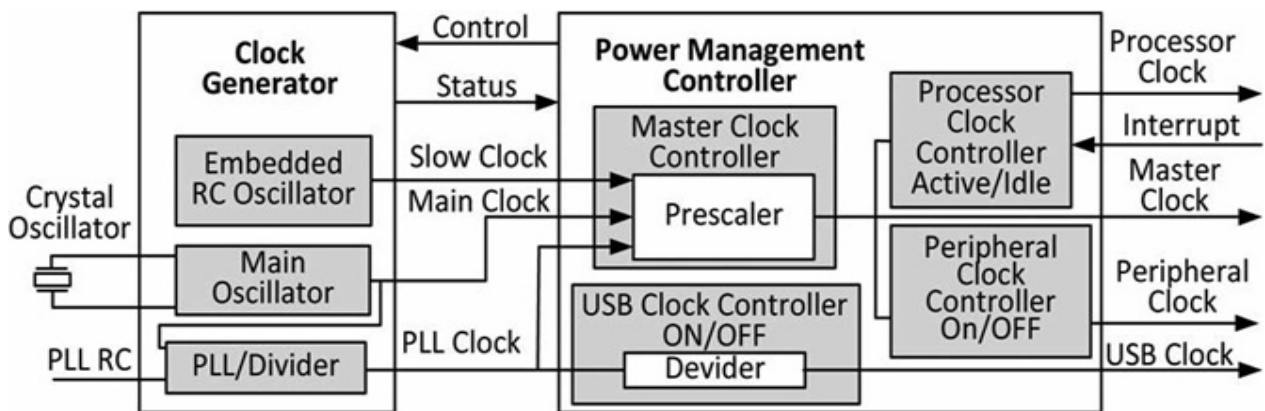
## III. ENERGY MANAGEMENT SECTION

To accomplish the power consumption, DVFS and DPM have been successfully used. DVFS varies the voltage of each part and also varies the frequency based on the system workload and other I/O devices. DPM selectively switch off the system elements while they are in idle mode. Only AT91SAM7x supports DPM (however, it controls only the processor and peripheral clocks) and cannot abuse DVFS (i.e. it doesn't provide variable supply voltage to its processor

core and I/O devices). Below we explained that how DPM is implemented (As it exists in many COTS microcontrollers), later we explained briefly the a methodology for employing DVFS technique to the microcontrollers, which are not equipped with DVFS features.

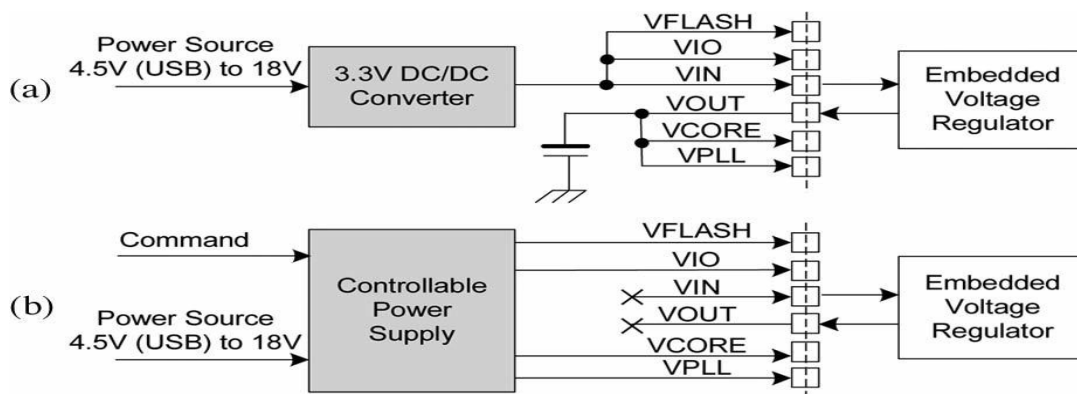
**A. DPM**

The AT91SAM7x enhances power consumption of the components by controlling (enabling/disabling or scaling) the clock of processor and I/O devices. In the below block diagram the power management controller is shown. The clock outputs are used to provide clocks to the processor, USB, I/O devices, and to master clock, the master clock is the clock which is provided to the memory controller and all the I/O devices. As shown in the fig.2, the master clock is generated by scaling any one of the clocks supplied by the clock generator. By giving a low frequency clock to the whole system by choosing the slow clock, or by selecting the main clock the power drop across PLL may be evaluated or power consumption of PLL can be saved.



**Fig. 2 Clock Generator and Power Management section.**

To save the processor power consumption it should be turned off by its clock, while it stands in idle mode and wait for an interrupts. It will help to save the sufficient amount of power. The processor clock restarts automatically by getting an interrupt or by resetting the device. To reduce the power consumption of each I/O devices, the operator can independently enable and disable the I/O devices clock by monitoring the master clock on each I/O devices with the help of I/O devices clock controller.



**Fig. 3 Power supply Section.**

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- (a) Typical power supply.
- (b) Proposed controllable power supply.

## B. DVFS

Normally DPM has two operational states only for systems components, viz. active state and idle state. To determine the active power consumption of components whose clock is enabled, the following equation is provided. Which include components operating frequency and supply voltage,.

$$P_{Active} = L_{Leakage} V + C_{eff} V^2 f$$

Where  $L_{Leakage}$  is the static leakage power and  $C_{eff} V^2 f$  is the dynamic power consumption ( $C_{eff}$  is the effective switched capacitance). To remove the dynamic power consumption we need to put the component into the mode by deactivating the clock. By specific hardware support and underneath software control, frequency scaling for system components can be used to exploit idle times for saving the power. The active power consumed by executing a task with  $N$  cycles at frequency  $f$  can be calculated as  $P_{Active} N / f$ . Which has a good result, on the static leakage power consumption as it remain unaffected although frequency scaling reduces the dynamic power consumption linearly. Besides, the consumed static power for a given computation increases due to increasing the task execution time when reducing the clock frequency. Henceforth, reduced power consumption can't be completed by frequency scaling alone. Frequency scaling can be effective only when employed in combination with voltage scaling. Voltage scaling techniques provides software controlled variable voltage regulators to establish the supply voltage of the processor core and active clock components. Clock generators and voltage regulators which are controlled by software allow the system to use DVFS. The main concept of behind DVFS techniques is to evaluate the minimum frequency that fulfills all timing constraints and then to vary the lowest possible voltage that allows this speed. Considering a linear relationship between frequency and voltage, the combined effects of voltage and frequency scaling result in reducing the active power consumption proportional to  $V^3$  and minimizing the energy consumption proportional to  $V^2$ . So, by scaling both the voltage and frequency, the power can be considerably minimize. This achievement does not come for free because a tradeoff exists between speed and power consumption. The AT91SAM7x microcontrollers have six power supply pins and a built-in voltage regulator, allowing the device to upkeep a 3.3-V single supply mode. Power provisions of the power supply pins are shown in Table I. Fig 3 shows the diagram of a typical single power supply mode where the 3.3-V power is supplied via a dc/dc voltage converter to VFLASH, VIO, and VIN. The input of the built-in voltage regulator is connected to the 3.3-V voltage source and output (i.e., the VOUT pin) supplies 1.8-V static voltage for the VCORE and VPLL pins. As Table I. shows, the USB transceiver, Flash memory, and I/O lines power supply range between 3.0 to 3.6 V, and in furthermore, the processor core and PLL power supply range between 1.65-1.95 V. This provides the opportunity for the device to differ the supply voltage rather than using just a single static voltage.

Pin name	Description	Range	Nominal
VFLASH	USB transceiver and flash	3.0-3.6V	3.3V
VIO	I/O lines	3.0-3.6V	3.3V
VIN	Voltage regulator and ADC	3.0-3.6V	3.3V
VOUT	Voltage regulator output	-	1.8V
VCORE	Processor core	1.65-1.95V	1.8V
VPLL	Oscillator and PLL	1.65-1.95V	1.8V

Table I Power Requirements in AT91SAM7x

In summary, to dynamically scale the supply voltage of a power pin of the microcontroller at run time, a digital code indicating the resistor and its desired value is loaded by the microcontroller into the digital potentiometer; after

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changing the adjustment resistor, the voltage regulator's output is scaled and set to the desired voltage value. Therefore, by the use of the proposed architecture, at run time, the microcontroller can dynamically set the voltage of the I/O devices and the processor core power pins. Generally, the proposed technique can be used to provide scalable voltages for the COTS devices that their supply voltage can vary within a range.

## VII. CONCLUSION

This paper has presented an innovative embedded system which includes two ARM7 microcontrollers, with separate power supply. This system is good for measuring the embedded systems with low power consumption and fault tolerance detection. In this system, we applied DVFS features to whole microcontroller (including the processor core, PLL, memory, and I/O). Hardware setup shows that applying DVFS to the whole microcontroller is more effective in reducing power consumption compared with applying DVFS only to the processor core or using power-down policies which are preferred by many embedded processors designer. Also, the system is furnished with accurate power measurement units, debugging ports; also provide facilities to evaluate fault-tolerance techniques. However the system is designed for ARM-based microcontrollers, it can also be used on other COTS devices,

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